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Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

1. Your reference GBP83730

2.

0107212.3

3 Full name, address and postcode of the or of each applicant (underline all surnames)



22 MAR 2001

Automatic Parallel Designs Limited
26A Binswood Avenue
Leamington Spa
Warwickshire CV32 5SQ

Patents ADP number (if you know it)

If the applicant is a corporate body, give the country/state of its incorporation

United Kingdom

4. Title of the invention A Multiplication Logic Circuit

5. Name of your agent (if you have one)

"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)

Marks & Clerk

57 - 60 Lincolns Inn Fields
London WC2A 3LS

Patents ADP number (if you know it)

18001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and (if you know it) the or each application number

Country

Priority application No
(if you know it)

Date of filing
(day / month / year)

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application

Date of filing
(day / month / year)

8. Is a statement of inventorship and of right to grant of a patent

required in support of this request? (Answer 'Yes' if:
a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

Yes

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Patents Form 1/77

Enter the number of sheets for any of the following items you are filing with this form.
Do not count copies of the same document

Continuation sheets of this form	0
Description	8
Claim(s)	2
Abstract	1
Drawing(s)	8

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8

10. If you are also filing any of the following, state how many against each item.

Priority documents

Translations of priority documents

Statement of inventorship and right to grant of a patent (Patents Form 7/77)

Request for preliminary examination and search (Patents Form 9/77)

Request for substantive examination (Patents Form 10/77)

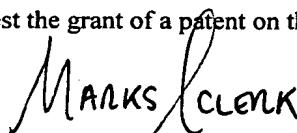
Any other documents (please specify)

1

11.

I/We request the grant of a patent on the basis of this application.

Signature



Date: 22 March 2001

12. Name and daytime telephone number of person to contact in the United Kingdom

GB Patent Filings

0207 400 3000

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**Statement of inventorship and of
right to grant of a patent**

The Patent Office

Cardiff Road
Newport
South Wales
NP9 1RH

1. Your reference	GBP83730	
2. Patent application number <i>(if you know it)</i>	0107212.3	
3. Full name of the or of each applicant	Automatic Parallel Designs Limited,	
4. Title of the invention	A Multiplication Logic Circuit	
5. State how the applicant(s) derived the right from the inventor(s) to be granted a patent	by employment	
6. How many, if any, additional Patents Forms 7/77 are attached to this form? <i>(see note (c))</i>		
7.	I/We believe that the person(s) named over the page <i>(and on any extra copies of this form)</i> is/are the inventor(s) of the invention which the above patent application relates to.	
	Signature	Date
	<i>Marks Clemin</i>	4 July 2001
8. Name and daytime telephone number of person to contact in the United Kingdom	GB Patent Filing section	0207 400 3000

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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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01955040001

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DUPPLICATE

A MULTIPLICATION LOGIC CIRCUIT

The present invention generally relates to digital electronic devices and more particularly to a multiplication logic circuit for multiplying two binary numbers.

It is instrumental for many applications to have a block that adds n inputs together. An output of this block is a binary representation of the number of high inputs. Such blocks, called parallel counters (L. Dadda, *Some Schemes for Parallel Multipliers*, Alta Freq 34: 349-356 (1965); E. E. Swartzlander Jr., *Parallel Counters*, IEEE Trans. Comput. C-22: 1021-1024 (1973)), are used in circuits performing binary multiplication. There are other applications of a parallel counter, for instance, majority-voting decoders or RSA encoders and decoders. It is important to have an implementation of a parallel counter that achieves a maximal speed. It is known to use parallel counters in multiplication (L. Dadda, *On Parallel Digital Multipliers*, Alta Freq 45: 574-580 (1976)).

A full adder is a special parallel counter with a three-bit input and a two-bit output. A current implementation of higher parallel counters i.e. with a bigger number of inputs is based on using full adders (C. C. Foster and F. D. Stockton, *Counting Responders in an Associative Memory*, IEEE Trans. Comput. C-20: 1580-1583 (1971)). In general, the least significant bit of an output is the fastest bit to produce in such implementation while other bits are usually slower.

The following notation is used for logical operations:

\oplus - Exclusive OR;

\vee - OR;

\wedge - AND;

\neg - NOT.

An efficient prior art design (Foster and Stockton) of a parallel counter uses full adders. A full adder, denoted FA, is a three-bit input parallel counter shown in figure 1. It has three inputs X_1, X_2, X_3 , and two outputs S and C. Logical expressions for outputs are

$$S = X_1 \oplus X_2 \oplus X_3,$$

$$C = (X_1 \wedge X_2) \vee (X_1 \wedge X_3) \vee (X_2 \wedge X_3).$$

A half adder, denoted HA, is a two bit input parallel counter shown in figure 1. It has two inputs X_1, X_2 and two outputs S and C. Logical expressions for outputs are

$$S = X_1 \oplus X_2,$$

$$C = X_1 \wedge X_2.$$

A prior art implementation of a seven-bit input parallel counter illustrated in figure 2.

Multiplication is a fundamental operation. Given two n-digit binary numbers

$$A_{n-1}2^{n-1} + A_{n-2}2^{n-2} + \dots + A_12 + A_0 \text{ and } B_{n-1}2^{n-1} + B_{n-2}2^{n-2} + \dots + B_12 + B_0,$$

their product

$$P_{2n-1}2^{2n-1} + P_{2n-2}2^{2n-2} + \dots + P_12 + P_0$$

may have up to $2n$ digits. Wallace has invented the first fast architecture for a multiplier, now called the Wallace-tree multiplier (Wallace, C. S., *A Suggestion for a Fast Multiplier*, IEEE Trans. Electron. Comput. EC-13: 14-17 (1964)). Dadda has investigated bit behaviour in a multiplier (L. Dadda, *Some Schemes for Parallel Multipliers*, Alta Freq 34: 349-356 (1965)). He has constructed a variety of multipliers and most multipliers follow Dadda's scheme.

Dadda's multiplier uses the scheme in on figure 3. If inputs have 8 bits then 64 parallel AND gates generate an array shown in figure 4. The AND gate sign \wedge is omitted for clarity so that $A_i \wedge B_j$ becomes $A_i B_j$. The rest of figure 4 illustrates array reduction that involves full adders (FA) and half adders (HA). Bits from the same column are added by half adders or full adders. Some groups of bits fed into a full adder are in rectangles. Some groups of bits fed into a half adder are in ovals. The result of array reduction is just two binary numbers to be added at the last step. One adds these two numbers by one of the fast addition schemes, for instance, conditional adder or carry-look-ahead adder.

UK patent application numbers 0019287.2 and 0101961.1 and US patent application number 09/637,532 and US patent application entitled "A parallel counter and a multiplication logic circuit" filed on 25 January 2001, the contents of all of which are hereby incorporated by reference, disclose a technique for the modification or deformation of the array prior to array reduction. The array deformation derives the benefit of reducing the depth of the array to a number greater than $2^{n-1}-1$ and less than or equal to 2^n-1 , where n is an integer. This reduction of the maximum depth of the array enables the efficient use of parallel counters in the array reduction step.

It is an object of the present invention to provide improved multiplication logic circuit in which the speed of operation of the multiplication logic circuit is improved.

The present inventors have realised that in the array reduction step the use of maximal length parallel counters can significantly reduce wiring delays present in the prior art array reduction logic. The inventors have also however realised that the outputs of the maximum length parallel counters experience different gate delays. Thus in accordance with the present invention, in addition to the use of maximal length parallel counters in the array reduction step, the outputs of the maximal length parallel counters are input to reduction logic circuits with asymmetric delays to ameliorate the effects of the differential delays of the output of the parallel counter circuits.

Thus in accordance with the present invention, outputs generated from the maximal length parallel counter logic that experience shorter delays are input to reduction logic inputs which incur longer delays in the generation of the output. Outputs of the maximal length parallel counter logic that experiences longer delays within the parallel counter logic are input to inputs of the asymmetric reduction logic which experience shorter delays in the generation of the output. Thus in this way the overall delays through the parallel counter logic and the further reduction logic are balanced and the differences in delays through the parallel counter logic is compensated for by the further reduction logic.

In accordance with the present invention, at least one maximal parallel counter is used in the array reduction step to reduce the array in one dimension by receiving all of the values in the array in one column

In a preferred embodiment of the present invention the array is modified by undergoing the array deformation as disclosed in copending UK applications numbers 0019287.2 and 0101961.1, US application number 09/637,532, and US application entitled "A parallel counter and a multiplication logic circuit" filed on 25 January 2001. Array deformation provides the benefit of reducing the number of inputs for a maximal column to a number greater than $2^{n-1}-1$ and less than or equal to 2^n-1 , where n is an integer. For example, for the multiplication of two 16 bit numbers, the array deformation process reduces the maximal depth of the array to 15 bits in any given column thereby enabling 15 bit input, 4 bit output parallel counters to be used in the first reduction step to reduce the array depth to a maximum of 4 bits. For a 32 bit input, the array deformation step reduces the maximal height of the array to 31 bits in any given column thereby enabling a 31 bit input, 5 output parallel counter to be used to provide an array of reduced depth which is a maximum of 5 bits.

In an embodiment of the present invention, the reduction logic with asymmetric delays comprises any combination of full adders, half adders and 4 to 2 compressors. Where a number of outputs from the parallel counters is 4 or more, 4 to 2 compressors are preferably used to generate 2 bit outputs.

Embodiments of the present invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of a full adder and a half adder in accordance with the prior art;

Figure 2 is a schematic diagram of a parallel counter using full adders in accordance with the prior art;

Figure 3 is a diagram of the steps used in the prior art for multiplication;
Figure 4 is a schematic diagram of the process of Figure 3 in more detail;
Figure 5 is a schematic diagram illustrating the structure of a generated deformed array in accordance with an embodiment of the present invention;
Figure 6 is a schematic diagram illustrating the array after reduction by maximal length parallel counters in accordance with an embodiment of the present invention;
Figure 7 is a diagram of the logic of a full adder showing the gate delays;
Figure 8 is a schematic diagram of a 4 to 2 compressor constructed from full adders in accordance with an embodiment of the present invention;
Figure 9 is a schematic diagram of the logic circuit for the second stage of the array reduction using 4 to 2 compressors in accordance with an embodiment of the present invention; and
Figure 10 is a diagram of the logic of a 4 to 2 compressor.

In the embodiment illustrated in Figure 5, the array generated in the process for multiplying two 16 bit binary numbers A and B is formed as a deformed array in accordance with the process disclosed in copending UK patent applications numbers 0019287.2 and 0101961.1, US patent application number 09/637,532 and a US patent application entitled "A parallel counter and a multiplication logic circuit" filed on 25 January 2001, the contents of which is hereby incorporated by reference. The advantage of this array over the array of the prior art as illustrated in Figure 4 is that the maximum number of bits in a column is smaller. In the prior art, for a 16 bit multiplication, a column will have 16 bits. The array of Figure 5 has four columns with 15 bits.

The first reduction step to reduce the array comprises the use of parallel counters to reduce each column from a maximum of 15 bits to 4 bits maximum as illustrated in Figure 6. Any conventional parallel counters can be used for reducing the maximal columns of 15 bits to 4 bits, although it is preferable to use the parallel counters disclosed in the copending applications identified above.

The 4 bits output from the parallel counters will have experienced different gate delays. Typically 2 outputs experience 4 gate delays and 2 outputs experience 5 gate delays. However, the use of a single logic circuit in the form of a maximal length parallel counter for the reduction of the array greatly reduces the wiring between circuits. There is thus a significant wiring benefit in using maximal length parallel counters.

Figure 7 is a logic diagram of a full adder that illustrates the asymmetric nature of the circuit. Inputs A and B can comprise outputs from a maximal length parallel counter which have experienced 4 gate delays and are therefore relatively advanced compared to the input to the circuit C which is an output from the maximal length parallel counter which has experienced 5 gate delays. Each gate delay in this example is expressed as an EXOR gate delay which is the slowest gate. And and OR gates are considered to have a relative delay of 0.5. Figure 7 illustrates the cumulative gate delay and as can be seen, the sum S is output with a cumulative gate delay of 6 and a carry C is also output with a cumulative gate delay of 6. Thus the full adder can be used as part of the second level of array reduction in order to compensate for the relative gate delays of the outputs of the maximal length parallel counters in the first level of array reduction.

Figure 8 is a schematic logic diagram of two adjacent 4 to 2 compressors each comprised of 2 full adders. The relative gate delays are illustrated to illustrate the asymmetric nature of the logic used as a second level of logic reduction in this embodiment of the present invention.

Figure 9 illustrates a chain of 4 to 2 compressors used to receive each of 4 columns of bits from the reduced array following the first level of reduction by the maximal length parallel counters. The output of the 4 to 2 compressors for each column comprises 2 bits. The 2 bits can then be added using conventional addition logic circuitry to generate the output binary number comprising a multiplication of the 2 n bit binary numbers.

Figure 10 is a logic diagram of the 4 to 2 compressor in accordance with an embodiment of the present invention.

Thus in this embodiment of the present invention an array is generated and modified by array deformation in accordance with the applicant's earlier inventive array modification technique. The array is reduced in two stages. The first stage is built upon the recognition that the wiring of the multiplication logic circuit can be reduced if a single parallel counter is used for the reduction of each column of the array. This however results in outputs which have suffered differential gate delays. Thus the invention ameliorates this problem by using a second level of array reduction which uses logic circuits for which the inputs experience relative differential gate delays i.e., the logic circuit imposes asymmetric delays on the inputs. In this way the relative delays caused by the use of the maximal length parallel counters does not cause a delay in the further reduction step.

Thus this multiplication logic circuit is highly efficient since it has reduced wiring and increase speed because of the balancing of the gate delays in the logic circuit.

Although the present invention has been described hereinabove with reference to a specific embodiment, it will be apparent to a skilled person in the art that modifications lie within the spirit and scope of the present invention.

For example, although the present invention has been described hereinabove with reference to a specific example in which the array is deformed before array reduction, the present invention is applicable to the reduction of an undeformed array. For example, the array can be generated using any prior art technique and can include the use of Booth encoding for the array generation step.

In the present invention any prior art parallel counter logic circuit can be used for the first level of the array reduction. Parallel counters can be used for any number of the columns that need not be used for all columns. For example, for the columns with three

bits, a full adder can be used. It may also be desirable for some columns to use full adders rather than the parallel counter. The number of columns reduced by the use of parallel counters is a design choice. It is however envisaged that it is preferable to use parallel counters for any columns having more than 3 bits in the array.

In accordance with the present invention, the second array reduction step can be implemented by any suitable logic for which there are differential delays experienced by the inputs in the generation of the outputs.

Although in the present invention any form of parallel counter can be used, in a preferred embodiment, the parallel counters disclosed in UK patent applications numbers 0019287.2 and 0101961.1; US patent application number 09/637,532 and a US patent application entitled "A parallel counter and a multiplication logic circuit" filed on 25 January 2001 are used.

In the present invention any conventional method can be used for the final step of addition of the two binary numbers in order to generate the output of the multiplication logic circuit.

CLAIMS:

1. A multiplication logic circuit for multiplying two n bit binary numbers, the circuit comprising:

array generation logic for performing the logical AND operation between each bit in one binary number and each bit in the other binary number to generate an array of logical AND combinations comprising an array of binary values;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the binary numbers;

wherein the array reduction logic comprises:

first array reduction logic comprising a plurality of binary counters, each for receiving the binary values of all binary numbers in a respective column of the array, and for outputting binary numbers; and

second array reduction logic having logic imposing asymmetric delays on inputs to the logic and for receiving the binary numbers output from the parallel counters at the inputs and for outputting said binary numbers to said addition logic.

2. A multiplication logic circuit according to claim 1, wherein said first array reduction logic includes adder logic for adding binary values of binary numbers in respective columns.

3. A multiplication logic circuit according to claim 2, wherein said adder logic comprises at least one full adder.

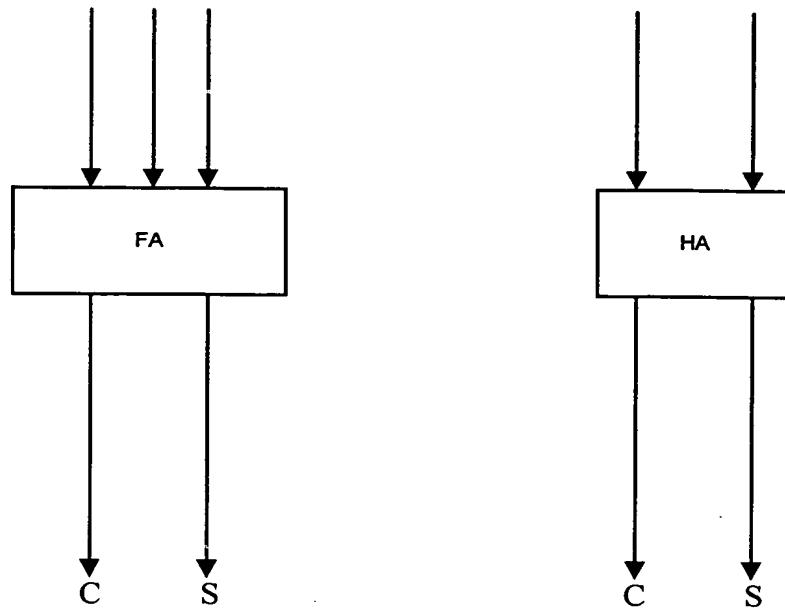
4. A multiplication logic circuit according to claim 2 or claim 3, wherein said adder logic is arranged to add binary values of binary numbers for columns in said array having 3 or less bits.

5. A multiplication logic circuit according to any preceding claim, wherein said second array reduction logic comprises any one of or combination of a full adder, a half adder, and four to two compressor logic.

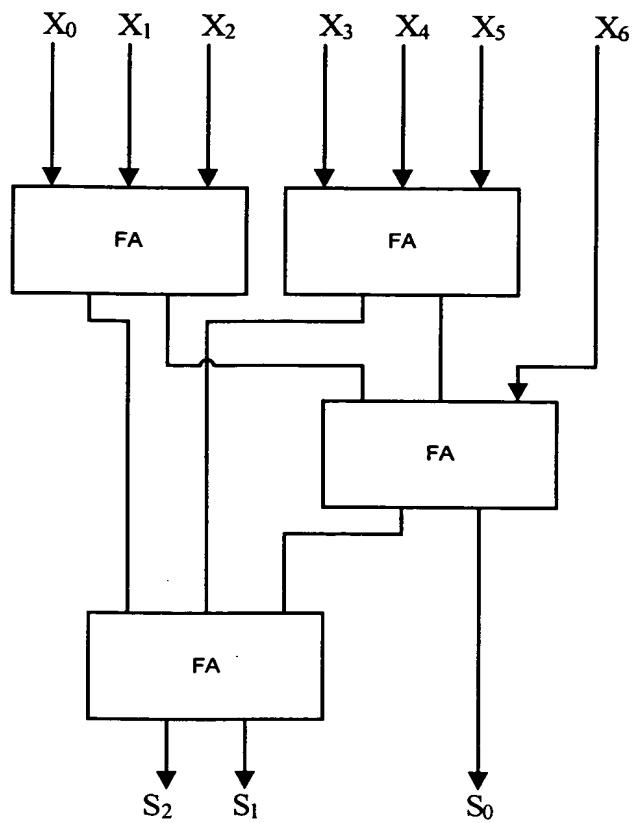
ABSTRACT:A MULTIPLICATION LOGIC CIRCUIT

A multiplication logic circuit comprises array generation logic and array reduction logic. The array reduction logic comprises array reduction logic for a first level of array reduction which comprises maximal length parallel counters for reducing maximal length columns. The output of the maximal length parallel counters are then further reduced by a second level of reduction logic comprising logic circuits with asymmetric delays in order to compensate for the differential delays experienced by the outputs of the maximal length parallel counters.

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PRIOR ART**Fig 1**

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PRIOR ART**Fig 2**

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PRIOR ART

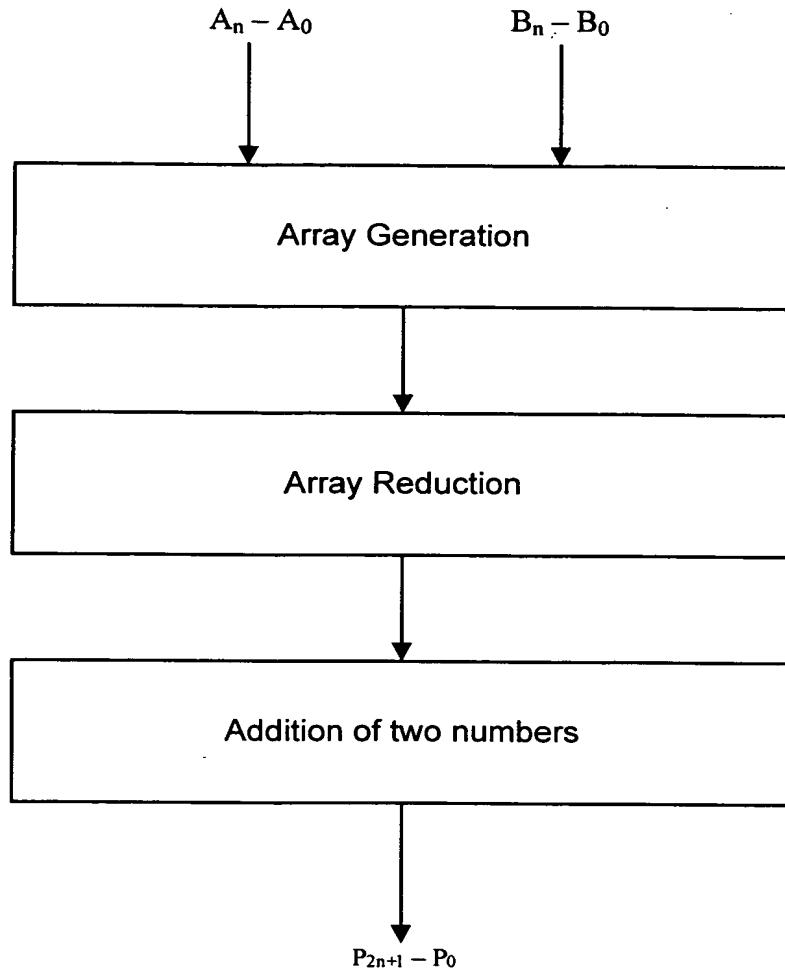


Fig 3

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PRIOR ART

$A_7B_0 \ A_6B_0 \ A_5B_0 \ A_4B_0 \ A_3B_0 \ A_2B_0 \ A_1B_0 \ A_0B_0$
 $A_7B_1 \ A_6B_1 \ A_5B_1 \ A_4B_1 \ A_3B_1 \ A_2B_1 \ A_1B_1 \ A_0B_1$
 $A_7B_2 \ A_6B_2 \ A_5B_2 \ A_4B_2 \ A_3B_2 \ A_2B_2 \ A_1B_2 \ A_0B_2$
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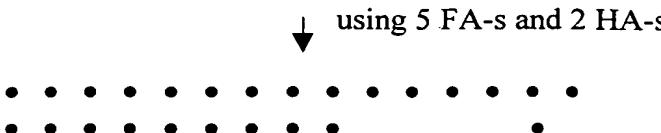
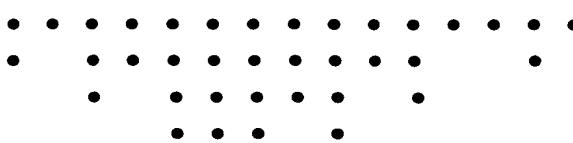
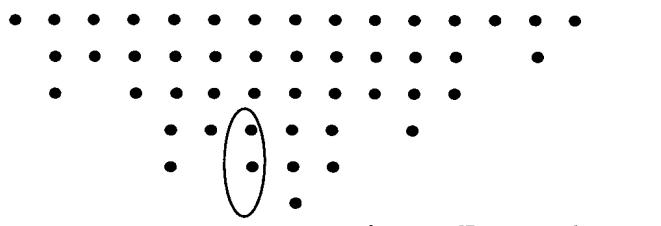
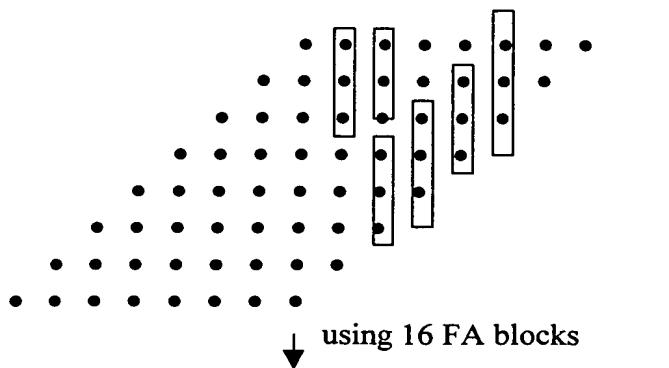


Fig 4

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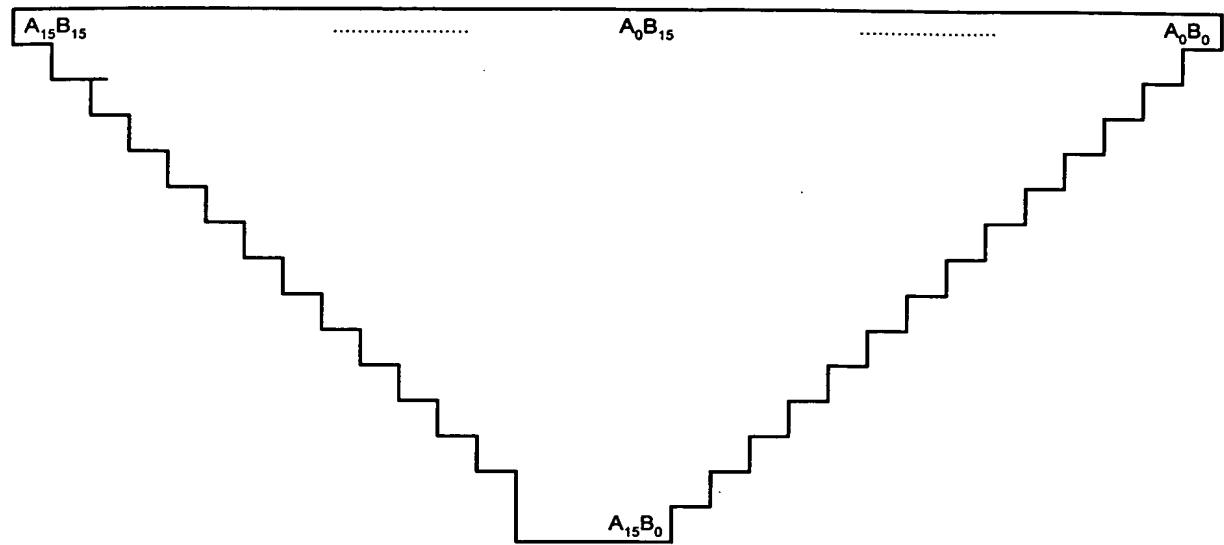


Fig 5

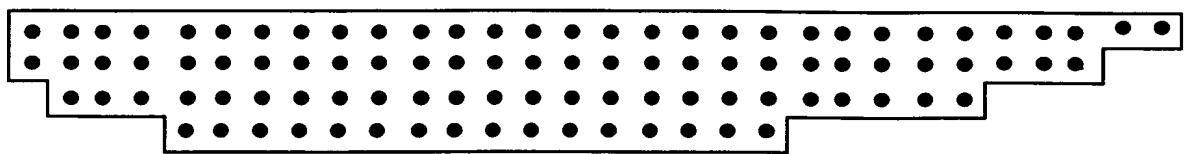


Fig 6

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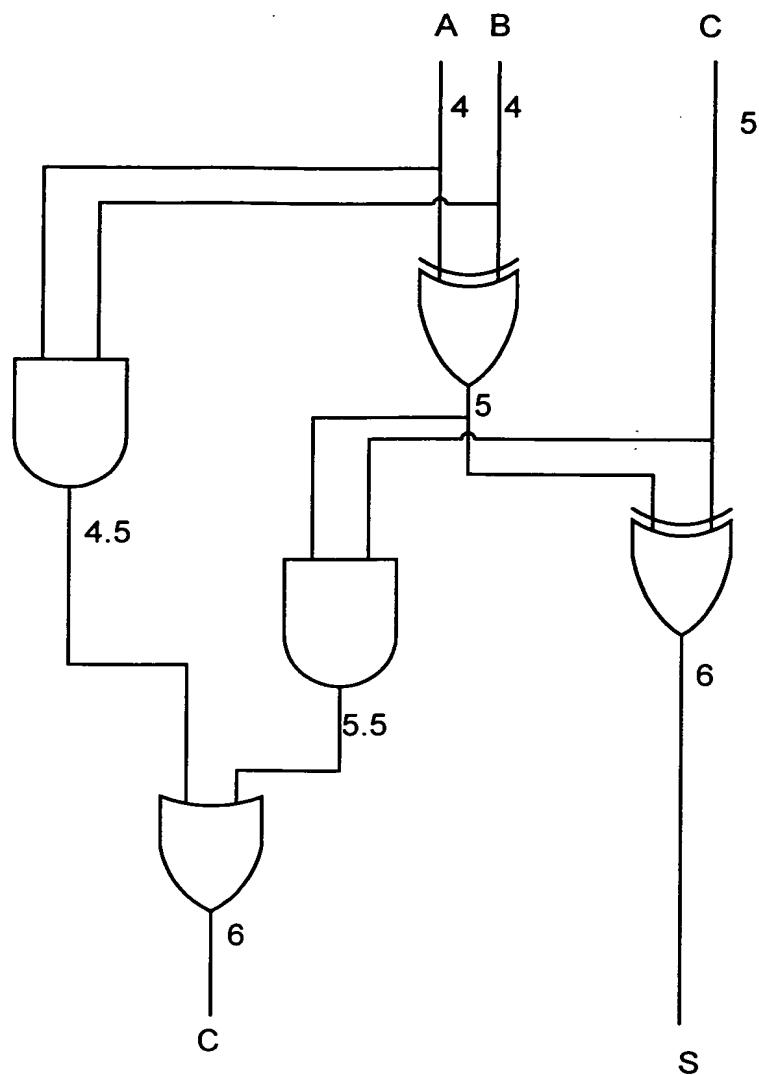


Fig 7

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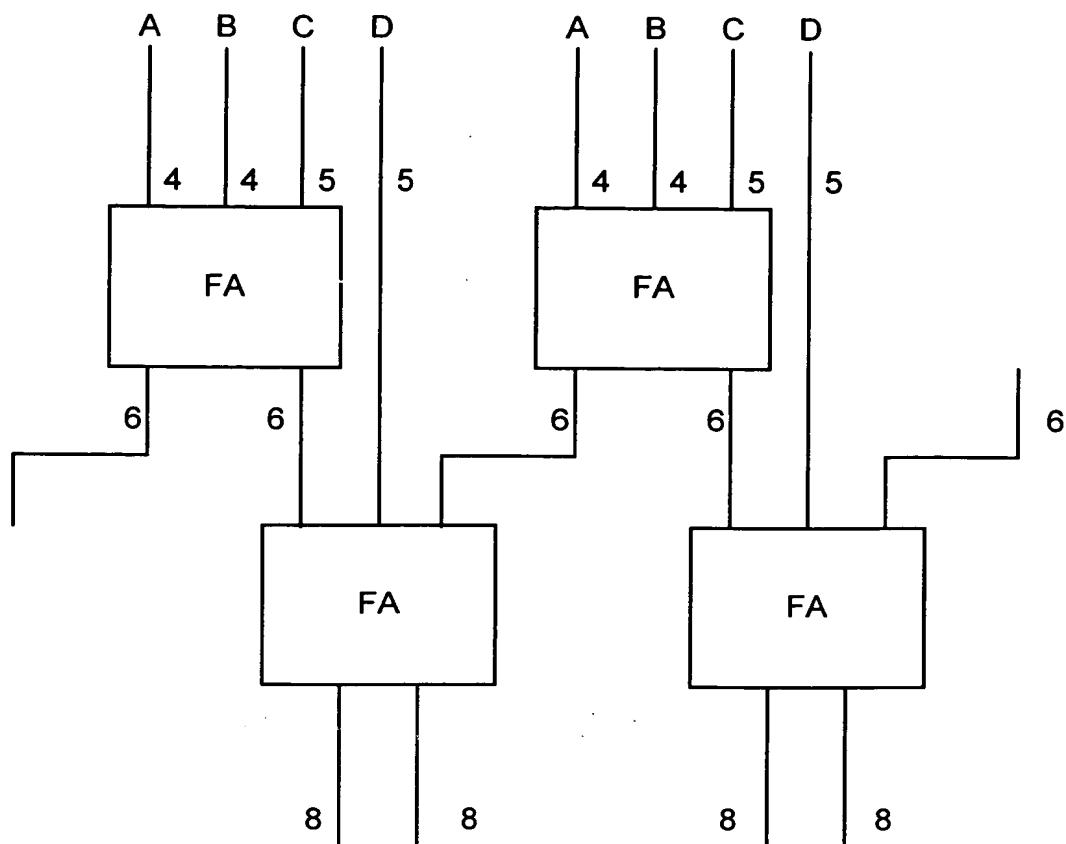


Fig 8

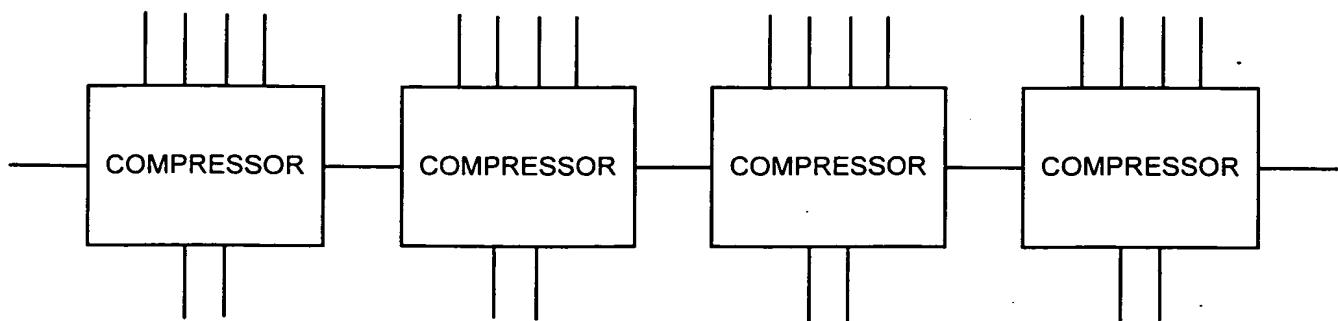


Fig 9

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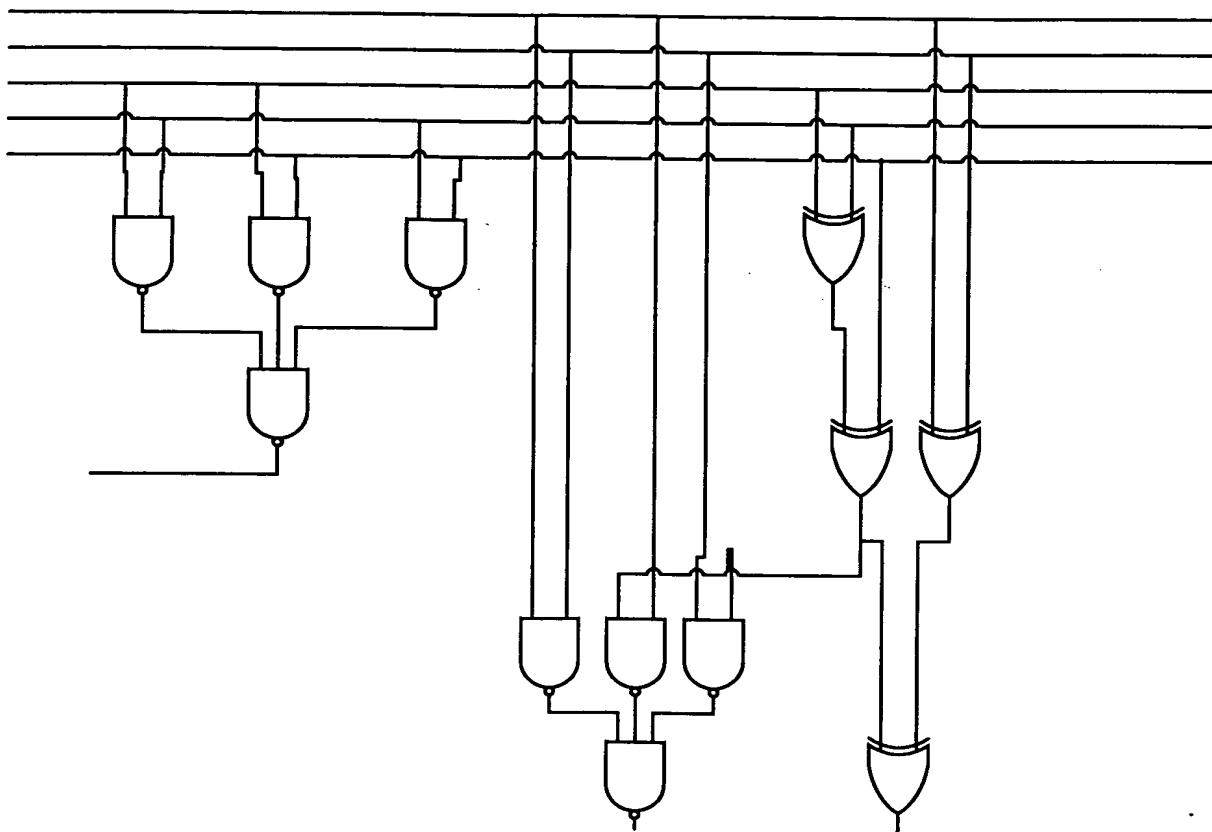


Fig 10

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